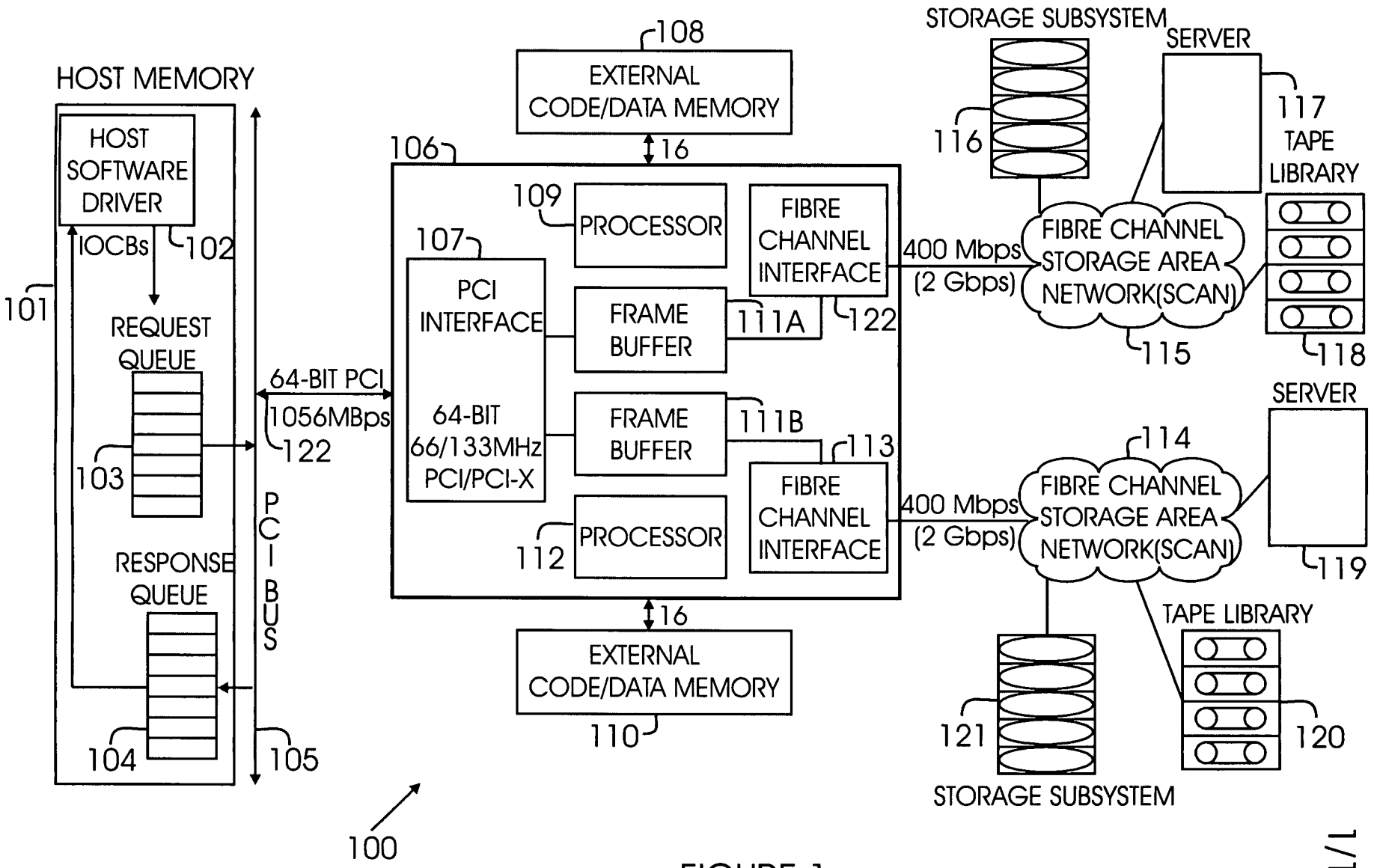

HOST MEMORY
HOST SOFTWARE DRIVER
IOCBs
102
101
REQUEST QUEUE
103
RESPONSE QUEUE
104
105
PCI BUS
64-BIT PCI
1056MBps
122
108
EXTERNAL CODE/DATA MEMORY
16
106
109
PROCESSOR
107
PCI INTERFACE
64-BIT 66/133MHz PCI/PCI-X
FRAME BUFFER
111A
FRAME BUFFER
111B
112
PROCESSOR
FIBRE CHANNEL INTERFACE
122
113
FIBRE CHANNEL INTERFACE
16
EXTERNAL CODE/DATA MEMORY
110
100
STORAGE SUBSYSTEM
116
SERVER
117
TAPE LIBRARY
400 Mbps
(2 Gbps)
FIBRE CHANNEL STORAGE AREA NETWORK(SCAN)
115
118
SERVER
114
FIBRE CHANNEL STORAGE AREA NETWORK(SCAN)
400 Mbps
(2 Gbps)
119
TAPE LIBRARY
121
120
STORAGE SUBSYSTEM

FIGURE 1

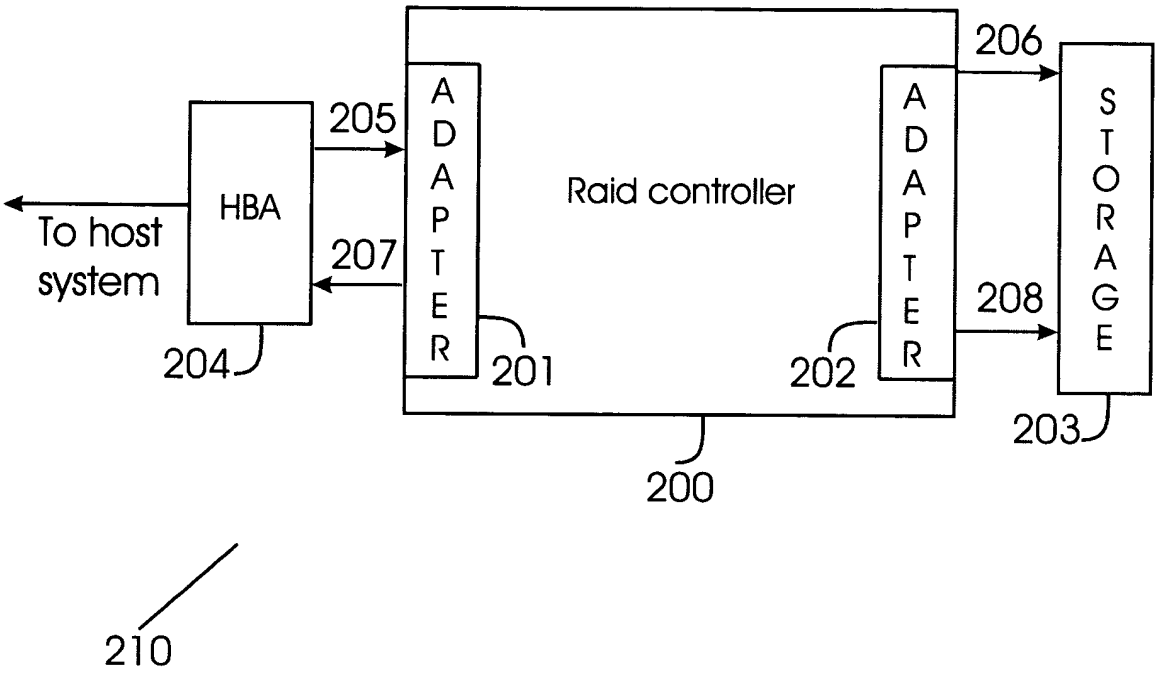


FIGURE 2A

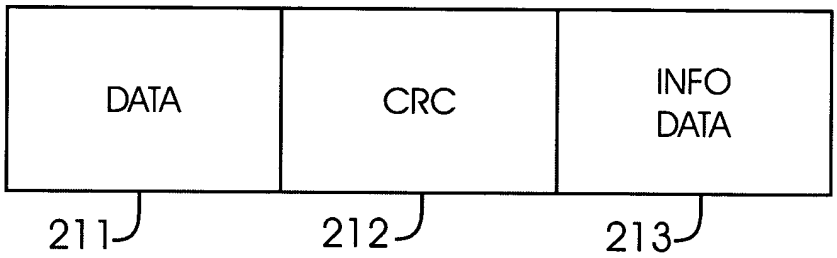
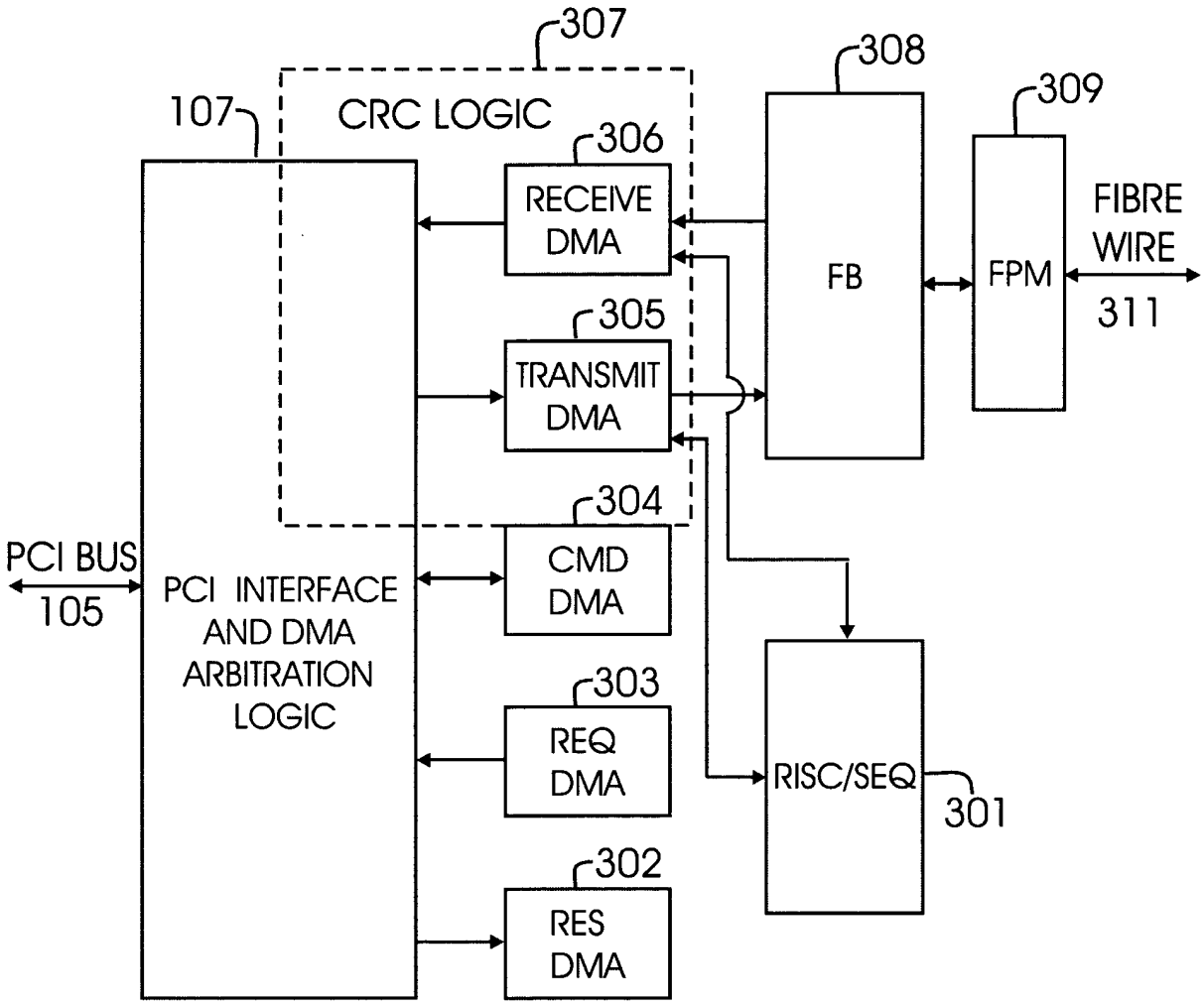


FIGURE 2B



SYSTEM BLOCK DIAGRAM

FIGURE 3

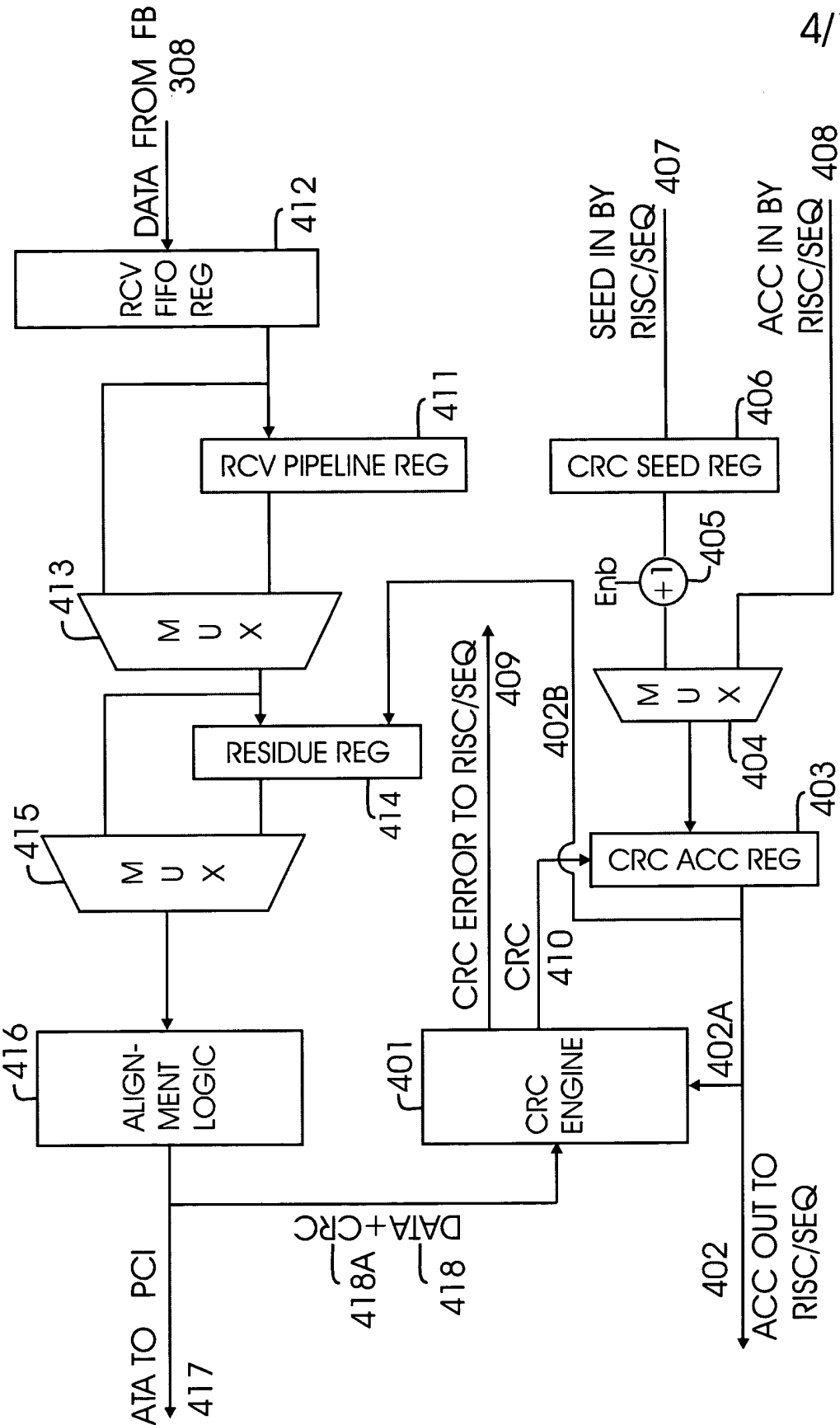

DATA FROM FB
308
RCV FIFO REG
412
RCV PIPELINE REG
411
SEED IN BY RISC/SEQ
407
CRC SEED REG
406
ACC IN BY RISC/SEQ
408
Enb
+1
405
M U X
413
RESIDUE REG
414
CRC ERROR TO RISC/SEQ
409
402B
M U X
404
M U X
415
CRC ACC REG
403
ALIGN-MENT LOGIC
416
CRC
410
CRC ENGINE
401
402A
DATA TO PCI
417
DATA+CRC
418A
418
402
ACC OUT TO RISC/SEQ
PCI RECEIVE PATH
400

FIGURE 4

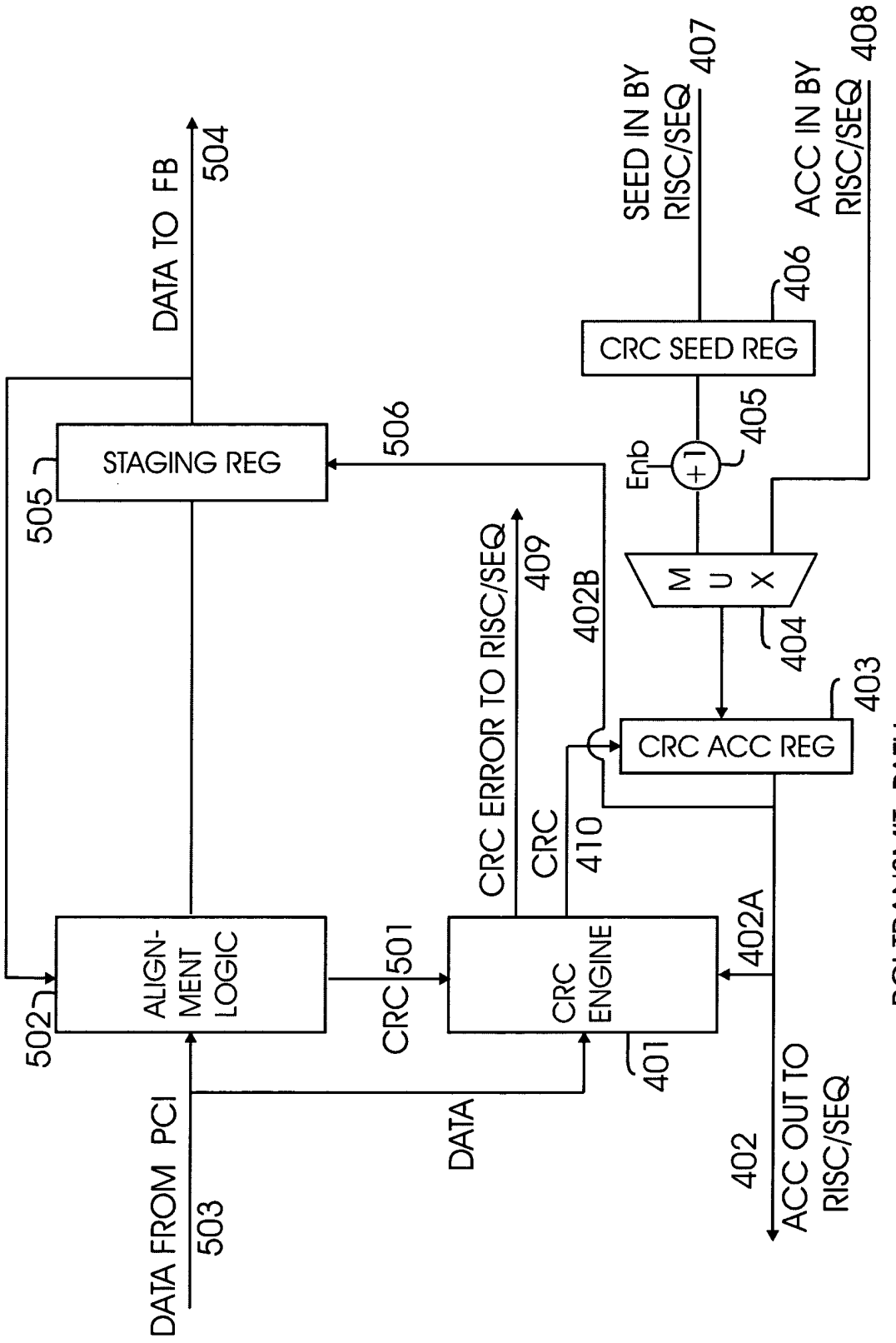

DATA FROM PCI
503
DATA
ALIGN-
MENT
LOGIC
502
CRC 501
CRC
ENGINE
401
402A
402
ACC OUT TO
RISC/SEQ
CRC ERROR TO RISC/SEQ
409
CRC
410
402B
CRC ACC REG
403
PCI TRANSMIT PATH
M
U
X
404
Enb
+1
405
CRC SEED REG
406
SEED IN BY
RISC/SEQ
407
ACC IN BY
RISC/SEQ
408
DATA TO FB
504
STAGING REG
505
506

FIGURE 5

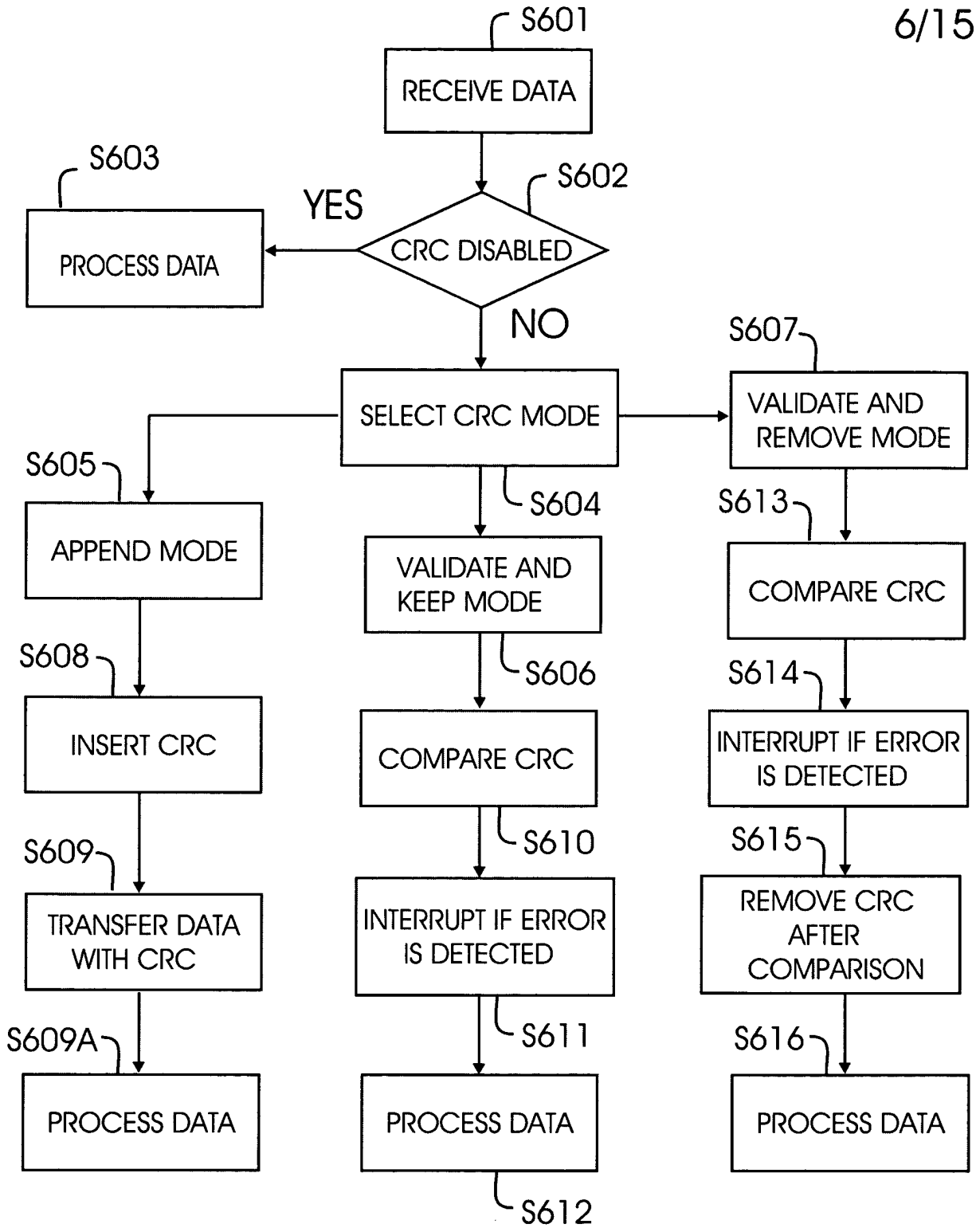

S601
RECEIVE DATA
S602
CRC DISABLED
YES
S603
PROCESS DATA
NO
SELECT CRC MODE
S605
APPEND MODE
S608
INSERT CRC
S609
TRANSFER DATA WITH CRC
S609A
PROCESS DATA
S604
VALIDATE AND KEEP MODE
S606
COMPARE CRC
S610
INTERRUPT IF ERROR IS DETECTED
S611
PROCESS DATA
S612
S607
VALIDATE AND REMOVE MODE
S613
COMPARE CRC
S614
INTERRUPT IF ERROR IS DETECTED
S615
REMOVE CRC AFTER COMPARISON
S616
PROCESS DATA

FIGURE 6

Receive DMA Register Map

RISC Address (h)	SEQ Address (h)	Register Name	Description
320 321 322 323	20 21 22 23	RDMA Address Counter 0 RDMA Address Counter 1 RDMA Address Counter 2 RDMA Address Counter 3	These registers reflect the current PCI address. They function as a 64-bit up counter, incrementing for each byte transferred across the PCI bus. This includes the CRC protection bytes.
324 325	24 25	RDMA Transfer Counter 0 RDMA Transfer Counter 1	These registers reflect the number of bytes remaining to be transferred across the PCI bus for a segment. This includes the CRC protection bytes.
326 327	26 27	RDMA Byte Counter 0 RDMA Byte Counter 1	These registers reflect the number of bytes remaining to be transferred across the PCI bus in the total RDMA transfer. This includes the CRC protection bytes.
328 329	28 29	RDMA Relative Offset 0 RDMA Relative Offset 1	These registers reflect the number of bytes received from the RD FIFO 412. This includes the CRC bytes in Validate_And _Keep mode. This does not include the CRC bytes in Append mode.
32A	2A	RDMA Control	Bit 14 : Reserved Bit 11-10 : Reserved Bit 6 :CRC Enable Bit 5 :CRC Register Select

I

FIGURE 7A-1

II

(I) (II)

32B	2B	RDMA Status	Bit 8 PCI Bus Error: Change in functionality. OR in Error conditions for CRC Error and Info Data Error.
32C 32D 32E 32F	2C 2D 2E 2F	RDMA Frame Counter RDMA Payload Byte Cntr RDS Low RDS High/ Error Enable	

The following values are multiplexed with DMA counters and are selectable by RDMA control register bit (e.g.5 ,in this case):

320 321	20 21	RDMA CRC Accumulator 0 RDMA CRC Accumulator 1	The firmware writes these registers when starting a RDMA transfer. The firmware reads this register on a context switch. The value read is restored when the context resumes. If the data transfer stops after CRC for Block 0 and before data for Block 1, these registers read back the CRC Seed Reload value for Block1. If the data transfer stops after data for Block 0 but before CRC for block 0, these registers read back CRC Value for Block 0.
322 323	22 23	CRC Seed Reload 0 CRC Seed Reload 1	These registers contain the CRC Seed Reload Value for the block being transferred. If the data transfer stops after CRC for Block 0 and before data for Block !, these registers read back CRC Seed Reload Value for Block 1.

(III) (IV)

FIGURE 7A-2

			If the data transfer stops after data for Block 0 but before CRC for Block 0, these registers read back CRC Seed Reload Value for Block 1. Once data transfer for Block 0 is done, there is no need to keep seed for Block 0. The next block transfer needs seed for block 1.
324	24	Block Byte Offset	This register contains the number of bytes remaining for a current block (down counter), and corresponds to the CRC Accumulator registers. If the data transfer stops after CRC for Block 0 and before data for Block 1, this register will read back a value equal to Block Size. If the data transfer stops after data for Block 0 but before CRC for Block 0, this register will read back a value of ZERO.
325 326	25 26	Info Data 0 Info Data 1	These registers contain the Info Data 213 value for the block being transferred. If a context switch occurs on a block boundary ,these registers should read back the Info Data 213 or the next block.
327	27	Disk CRC Configuration	This register contains the Disk CRC Configuration parameters. Bit 15: Select Last Block CRC Value For Read 0 : selects accumulator for current block 1 : selects accumulator for last block Bit 14:6 : Reserved Bit 6 : Disable CRC Validation

FIGURE 7A-3

(V) (VI)

			Bit 5: Increment CRC Seed. If this bit is set, the CRC seed increments from block to block. If this bit is not set , the CRC seed will be constant. Bit 4: Info Data Supported. If this bit is set Info Data 213 support is enabled. 8 bytes of protection data(CRC + Info Data) are appended to each block. If this bit is not set, only 4 bytes(CRC) are appended to each block. Bit 3 : Increment Info Data. If this bit is set, the Info Data 213 is incremented from block to block. If this bit is not set , the info data will remain constant. Bit 2 : Disable Info Data Validation. If this bit is set, the Info Data 213 is not validated. If this bit is reset, the 4 bytes of Info Data is compared against the expected value (maintained in the Info Data Registers). Bit 1 : CRC Protection Mode (applicable only in Disk CRC mode, iSCSI always does append) 0 : Append 1 : Validate and Keep Bit 0 : CRC Mode Select 0 : Disk CRC 1 : iSCSI CRC
328	28	Disk Block Size	Bits 15-12 : Reserved Bits 11-0 : Block Size(Bits1:0 can be ignored).Supported block sizes are from 4 bytes to 0xFFC bytes.

(VII) (VIII)

FIGURE 7A-4

(VII) (VIII)

329-32 A	29-2A	Reserved	
32B	2B	CRC STATUS	Bits 15-2 : Reserved Bits 1 : CRC Error (Validate And Keep mode only) Bits 0 : Info Data Error (Validate And Keep mode only) PCI Bus Error, bit 8 in DMA Status register is also set to 1 when any of the error status bits in CRC Status register are set.
32C-32F	2C-2F	Reserved	

FIGURE 7A-5

RISC Address	SEQ Address	Register Name	Description
90 91 92 93	20 21 22 23	TDMA Address Counter 0 TDMA Address Counter1 TDMA Address Counter 2 TDMA Address Counter 3	These registers reflect the PCI address. They function as a 64- bit up counter, incrementing for each byte transferred across the PCI bus. This includes the CRC protection bytes.
94 95	24 25	TDMA Transfer Counter 0 TDMA Transfer Counter 1	These registers reflect the number of bytes remaining to be transferred across the PCI bus for a segment. This includes the CRC protection bytes.
96	26	TDMA byte Counter 0	These registers reflect the number of bytes remaining

(IX) FIGURE 7B-1 : TDMA Register Map (X)

IX

X

97	27	TDMA byte Counter 1	to be transferred across the PCI bus in the total TDMA transfer. This includes the CRC protection bytes.
98 99	28 29	TDMA Relative offset 0 TDMA Relative offset 1	These registers reflect the number of bytes transferred to the TD FIFO. This includes the protection bytes in Validate_And_ Keep mode. This does not include the protection bytes in Validate_ And_Remove mode.
9A	2A	TDMA Control	Bit 14: Resvered Bit 11- 10: Resvered Bit 6 :CRC Enable Bit 5 :CRC Register seclect
9B	2B	TDMA Status	Bit 8 PCI Bus Error: Change in functionality. Or in Error conditions for CRC Error and Info Data Error;.
9C 9D 9E 9F	2C 2D 2E 2F	TDMA Frame Byte Counter TDMA Payload Byte Size Resvered Resvered	

The following register values are multiplexed with DMA counters and are selectable via TDMA control register bit (for example, bit 5).

90 91	20 21	TDMA CRC Accumulator 0	The firmware writes these registers when starting a TDMA tranfer.

XI

XII

FIGURE 7B-2

(XI) (XII)

		TDMA CRC Accumulator 1	If the data transfer stops after CRC for Block 0 and before data for Block 1, these registers read back the CRC Seed Reload Value for Block 1. If the data transfer stops after data for Block 0 but before CRC for Block 0 . These registers will read back CRC value for Block 0.
92 93	22 23	CRCSeed Reload 0 CRCSeed Reload 1	These registers contain the CRC Seed Reload Value for the block being transferred. If the data transfer stops after CRC for Block 0 and before data for Block 1, these registers read back CRC Seed Reload Value for Block 1. If the data transfer stops after data for Block 0 but before CRC for Block 0, these registers read back CRC Seed Reload Value for Block 0.
94	24	Block byte offset	This register contains the number of bytes remaining for the current block (down counter), and corresponds to the CRC Accumulator registers. If the data transfer stops after CRC for Block 0 and before data for Block 1, this register reads back a value equal to Block Size. If the data transfer stops after data for Block 0 but before CRC for Block 0, this register reads back a value of ZERO.

(XIII) (XIV)

FIGURE 7B-3

XIII

XIV

95 96	25 26	Info Data 0 Info Data 1	These registers contain the Info Data 213 value for the block being transferred. If a context switch occurs on a block boundary, these registers should read back the Info Data for the next block.
97	27	Disk CRC configuration	This register contains the Disk CRC configuration parameters. Bit 15: Selects last block CRC Value For Read 0: selects accumulator for current block 1: selects accumulator for last block. Bit 14:7: Reserved Bit 6: Disable CRC Validation Bit 5: Increment CRC seed. If this bit is set, the CRC seed increments from block to block. If this bit not set, the CRC seed will be constant. Bit 4: Info Data supported.If this bit is set, Info Data support is enabled. 8 bytes of protection data(CRC +Info Data) are validated on each block.If this bit not set.only 4 bytes (CRC)are validated on each block. Bit 3: Increment Info Data, If this bit is set, the Info Data 213 increments from block to block. If this bit is not set, the Info data will remain constant. Bit 2: Disable Info Data Validation. If this bit is set, the Info Data

XV

XVI

FIGURE 7B-4

			213 is not validated. If this bit is reset, the 4 bytes of Info Data 213 are compared against the expected value (maintained in the Info Data registers). Bit 1: CRC Protection Mode (applicable only in Disk CRC mode iSCSI always does Validate And Remove) 0 : Validate And Remove 1: Validate And Keep Bit 0 : CRC Mode Select 0 : Disk CRC 1 : iSCSI CRC
98	28	Disk Block Size	Bits 15-12 : Reserved Bits 11-0 : Block Size (Bits 1:0 can be ignored.) Supported Block sizes are from 4 bytes to0xFFC byte
99-9A	29-2A	Reserved	
9B	2B	CRC Status	Bits 15-2 : Reserved Bits 1 : CRC Error Bits 0 : Info Data Error Note : PCI Bus Error, bit 8 in DMA Status register is also set to 1 when any of the error status bits in CRC Status register are set.)
9C-9F	9C-9F	Reserved	

FIGURE 7B-5